

REMARKS

By the present Amendment, claims 3, 20, 21, and 25 have been amended to more appropriately define the present invention. Applicant submits that no new matter has been added.

Claims 3, 12, 13, and 19-25 are currently under consideration, with claims 1, 2, 4-11, and 14-18 being withdrawn from consideration as directed to a non-elected invention. In the Office Action, the Examiner objected to the Specification; rejected claims 3, 12, 13, 19, and 20 under 35 U.S.C. § 112, second paragraph; rejected claims 21-24 under 35 U.S.C. § 102(e) as being anticipated by Sakui et al. (U.S. Patent No. 6,239,495); rejected claims 3, 12, 13 and 19 under 35 U.S.C. § 103(a) as unpatentable over Sakui et al. in view of Iijima et al. (U.S. Patent No. 5,729,439); rejected claims 3, 12, 13, and 19 under 35 U.S.C. § 103(a) as being unpatentable over Sakui et al. in view of Komiyama (U.S. Patent No. 6,424,050); and rejected claims 20 and 25 under 35 U.S.C. § 103(a) as being unpatentable over Sakui et al. and Iijima et al. further in view of Hsuan et al. (U.S. Patent No. 6,236,109).

Applicant wishes to thank Examiner Im and Examiner Lee for allowing Applicant's representatives to discuss the pending claims during a personal interview on February 19, 2004. The substance of the interview is summarize as follows:

Applicant's representatives explained the recitations of the pending claims. Specifically, Applicant's representatives pointed out to the Examiners that claims 3 and 20 were amended in the Amendment filed on October 29, 2003 to clarify the recitations of those claims. Aided by the explanation, the Examiners requested Applicant to amend claims 3 and 20 to restore the language from before the last Amendment to overcome the objection to the Specification and the rejection of the claims under 35 U.S.C. § 112,

second paragraph. Applicant has amended claims 3 and 20 to comply with the Examiners' request. Applicants representatives further discussed the patentability of the pending claims over the cited references.

Objection to the Specification

As discussed during the interview on February 19, 2004, Applicant has amended claims 3 and 20 to restore the language from before the Amendment filed on October 29, 2003. Accordingly, Applicant deems the objection to the Specification overcome and respectfully requests the Examiner to withdraw the objection to the Specification.

Rejection of claims

Applicant respectfully traverses the rejections of claims 3, 12, 13, and 19-25, as detailed above, for the following reasons.

Rejection under 35 U.S.C. § 112, second paragraph

On pages 2-3 of the Office Action, the Examiner rejected claims 3, 12, 13, 19, and 20 under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention.

As discussed during the interview on February 19, 2004, Applicant has amended claims 3 and 20 in accordance with the Examiner's request to restore the language from before the Amendment filed on October 29, 2003. Accordingly, Applicant deems the rejection of the present claims 3, 12, 13, 19, and 20 under 35 U.S.C. § 112, second paragraph overcome, and respectfully requests the Examiner to allow these claims.

Rejection under 35 U.S.C. § 102()

Applicant respectfully traverses the rejection of claims 21-24 under 35 U.S.C. § 102(e) as being anticipated by Sakui et al. for the following reasons.

In order to properly anticipate Applicant's claimed invention under 35 U.S.C. § 102(e), the Examiner must show that each and every element of each of the claims in issue is found, either expressly described or under principles of inherency, in a single prior art reference. Furthermore, "[t]he identical invention must be shown in as complete detail as is contained in the ... claim." See M.P.E.P. §2131, page 2100-69, 8th Ed., August 2001, quoting *Richardson v. Suzuki Motor Co.*, 868 F.2d 1126, 1236, 9 U.S.P.Q.2d 1913, 1920 (Fed. Cir. 1989). Further, "the elements must be arranged as required by the claim." M.P.E.P. §2131, p. 2100-69.

Independent claim 21 recites a semiconductor device comprising, among other things, "a plurality of first connecting terminals ... a plurality of second connecting terminals ... and some of the first connecting terminals or the second connecting terminals are distributed and arranged substantially on an entire surface of the semiconductor chip, and power source supply potential or ground potential is to be applied to said some of the first or second connecting terminals."

In the Office Action, the Examiner alleges that Sakui et al. discloses "either the first connecting terminals [or] the second connecting terminals is distributed and arranged in the surface of the semiconductor chip, and power supply (V_{ss} ; a ground voltage) is to be applied on a portions of the bumps (bumps 8-1, 8-2, 8-3 of the first chip 12-1 in Fig. 3)." Office Action at page 9. Applicant respectfully disagrees.

Present independent claim 21 recites, in part, “some of the first connecting terminals or the second connecting terminals are distributed and arranged substantially on an entire surface of the semiconductor chip, and power source supply potential or ground potential is to be applied to said some of the first or second connecting terminals.” Fig. 3 of Sakui et al. discloses bumps 8-1 through 8-3 connected to a ground potential. However, Sakui et al. does not disclose at least some of the first connecting terminals or the second connecting terminals are distributed and arranged substantially on an entire surface of the semiconductor chip, and power source supply potential or ground potential is to be applied to said some of the first or second connecting terminals, as claimed. In other words, bumps 8-1 through 8-3 of Sakui et al. do not read on the claimed connecting terminals connected to a power supply or a ground potential at least because these terminals are not “distributed and arranged substantially on an entire surface of the semiconductor chip,” as recited in claim 21.

In summary, Sakui et al. does not disclose at least “a plurality of first connecting terminals ... a plurality of second connecting terminals ... and some of the first connecting terminals or the second connecting terminals are distributed and arranged substantially on an entire surface of the semiconductor chip, and a power source supply potential or ground potential is to be applied to said some of the first or second connecting terminals,” as recited in claim 21. Therefore, the rejection of claim 21 under 35 U.S.C. § 102(e) is improper and Applicant respectfully requests the Examiner to withdraw the rejection and the claim be allowed. Claims 22-24 are also allowable at least in view of their dependency from allowable claim 21.

Rejection under 35 U.S.C. § 103(a)

Applicant respectfully traverses the rejection of claims 3, 12, 13, 19, 20, and 25 under 35 U.S.C. § 103(a) because a *prima facie* case of obviousness has not been established by the Examiner.

In order to establish a *prima facie* case of obviousness, three basic criteria must be met. First, the prior art reference (or references when combined) must teach or suggest all the claim elements. Second, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify a reference or to combine reference teachings. Third, there must be a reasonable expectation of success. See M.P.E.P. § 2143.

I. Claims 3, 12, 13, and 19 (Sakui et al. and Iijima et al.)

On pages 2-4 of the Office Action, the Examiner rejected claims 3, 12, 13, and 19 under 35 U.S.C. § 103(a) as being unpatentable over Sakui et al. in view of Iijima et al.

Claim 3 recites a semiconductor device comprising, among other things, “a plurality of first connecting terminals ... a plurality of second connecting terminals ... and one of the first connecting terminals and the second connecting terminals are arranged to be closer to [an] assembly board and the average density of arrangement of the one of the first connecting terminals and the second connecting terminals is lower than that of another of the first connecting terminals and the second connecting terminals.”

In the Office Action, the Examiner alleges that “[i]n detail, Fig. 3 [of Sakui et al.] shows that the number of the second connecting terminals (7 metal bumps; 8-1 through 8-7) is more than that of the first connecting terminals (five metal bumps) which are

formed on the first surface of the chip 12-1.” Office Action at pages 3-4. As discussed during the interview on February 19, 2004, Applicant respectfully disagrees with the Examiner’s characterization of the claim language. In accordance with the Examiner’s request, Applicant has amended claim 2 to clarify the invention.

Present independent claim 3 recites “one of the first connecting terminals and the second connecting terminals are arranged to be **closer** to [an] assembly board and the average density of arrangement of **the** one of the first connecting terminals and the second connecting terminals is lower than that of another of the first connecting terminals and the second connecting terminals.” (emphasis added). Applicants point out that the recitation “the one of the first connecting terminals and the second connecting terminals” refers to the one of the first and second terminals that is arranged to be **closer to an assembly board**.

In contrast, Fig. 3 of Sakui et al. shows a connecting terminal layer with five bumps and another connecting terminal layer with seven bumps (8-1 through 8-7). If the Examiner is alleging that the bumps 8-1 through 8-7 correspond to the claimed “one of the ... terminals [that are] arranged to be closer to [an] assembly board,” then those bumps must also have a lower density of arrangement than the other connecting terminal layer (the one with five bumps), which is simply not true.

Therefore, contrary to the Examiner’s allegations, Sakui et al. does not teach or suggest at least “a plurality of first connecting terminals ... a plurality of second connecting terminals ... and one of the first connecting terminals and the second connecting terminals are arranged to be closer to [an] assembly board and the average density of arrangement of the one of the first connecting terminals and the second

connecting terminals is lower than that of another of the first connecting terminals and the second connecting terminals,” as recited in claim 3.

Iijima et al., cited merely to show a flip-chip arrangement, fails to cure the deficiencies of Sakui et al., as noted above. Therefore, Sakui et al. and Iijima et al., either taken alone or in combination, fail to teach or suggest at least “a plurality of first connecting terminals ... a plurality of second connecting terminals ... and one of the first connecting terminals and the second connecting terminals are arranged to be closer to [an] assembly board and the average density of arrangement of the one of the first connecting terminals and the second connecting terminals is lower than that of another of the first connecting terminals and the second connecting terminals,” as recited in claim 3.

Further, the Examiner alleges that “[i]t would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teaching of Iijima et al. to the device of Sakui et al to have a flip chip arrangement since a flip chip configuration provides a higher density and better performance for a device circuit.” Applicant disagrees with the Examiner’s allegations and conclusions as an unsubstantiated statement of questionable relevance to Applicant’s claimed invention. Applicant further refers the Examiner to the February 21, 2002 Memorandum from USPTO Deputy Commissioner for Patent Examination Policy, Stephen G. Kunin, regarding “Procedures for Relying on Facts Which are Not of Record as Common Knowledge or for Taking Official Notice.” In relevant part, the Memorandum states, “If the examiner is relying on personal knowledge to support the finding of what is known in the art, the examiner must provide an affidavit or declaration setting forth specific factual

statements and explanation to support the finding” (Memorandum, p. 3). Further, the Memorandum indicates that the Federal Circuit has “criticized the USPTO’s reliance on ‘basic knowledge’ or ‘common sense’ to support an obviousness rejection, where there was no evidentiary support in the record for such a finding.” Id. at 1.

Applicant submits that “[d]eficiencies of the cited references cannot be remedied by the Board’s general conclusions about what is “basic knowledge” or “common sense.”” In re Lee, 61 USPQ2d 1430, 1432-1433 (Fed. Cir. 2002), quoting In re Zurko, 59 USPQ2d 1693, 1697 (Fed. Cir. 2001). Should the Examiner maintain the rejection after considering the arguments presented herein, Applicants submit that the Examiner must provide “the explicit basis on which the examiner regards the matter as subject to official notice and [allow Applicants] to challenge the assertion in the next reply after the Office action in which the common knowledge statement was made” (Id. at 3, emphasis in original), or else withdraw the rejection.

Therefore, at least because Sakui et al. and Iijima et al., either taken alone or in combination, fail to teach or suggest each and every element of claim 3, the Examiner has failed to establish a *prima facie* case of obviousness for claim 3. Accordingly, the rejection of claim 3 is improper under 35 U.S.C. § 103(a), and Applicant respectfully requests the Examiner to withdraw the rejection of claim 3 and the claim allowed. Applicant submits that claims 12, 13, and 19 are also allowable at least in view of their dependency from allowable claim 3.

II. Claims 3, 12, 13, and 19 (Sakui et al. and Komiyama)

On pages 4-5 of the Office Action, the Examiner rejected claims 3, 12, 13, and 19 under 35 U.S.C. § 103(a) as being unpatentable over Sakui et al. in view of Komiyama.

As discussed above regarding the rejection of claim 3, Sakui et al. does not teach or suggest at least “a plurality of first connecting terminals ... a plurality of second connecting terminals ... and one of the first connecting terminals and the second connecting terminals are arranged to be closer to [an] assembly board and the average density of arrangement of the one of the first connecting terminals and the second connecting terminals is lower than that of another of the first connecting terminals and the second connecting terminals.”

Komiyama fail to cure these deficiencies of Sakui et al. Komiyama discloses a flip chip IC chip with a mounting surface that is externally exposed and is provided with external terminals 15. See id. at Fig. 4. The Examiner alleges that Komiyama “clearly show[s] that the density of the conductive bumps arrangement is different between the first connecting terminals 15 and the second connecting terminals 24, 49 of the first chip 1 in Fig. 4.” Office Action at page 5. Applicant respectfully disagrees. Without acceding to the Examiner’s characterization of Komiyama, if one were to accept, for argument’s sake, that terminals 15 correspond to the claimed “the one of ... terminals” that are closer to an assembly board, then still, it is not true that they have an average density of arrangement that is lower than the terminals 24 and 49 (as shown in Komiyama). As can be clearly seen from Fig. 4, terminals 15 are spaced closer than the terminals 24 and 29, and, therefore, are not of a lower average density of arrangement.

Therefore, Sakui et al. and Komiyama, either taken alone or in combination, do not teach or suggest at least “a plurality of first connecting terminals ... a plurality of second connecting terminals ... and one of the first connecting terminals and the

second connecting terminals are arranged to be closer to [an] assembly board and the average density of arrangement of the one of the first connecting terminals and the second connecting terminals is lower than that of another of the first connecting terminals and the second connecting terminals,” as recited in claim 3.

Further, the Examiner alleges that “[i]t would have been obvious to one of ordinary skill in the art at the time of the invention to utilize the teaching of Komiyama to have a different number of conductive bumps for two connecting terminals in a flip chip configuration in order to have more compact arrangement to reduce a device size.” Applicant disagrees with the Examiner’s allegations and conclusions as an unsubstantiated statement of questionable relevance to Applicant’s claimed invention. Applicant submits that “[d]eficiencies of the cited references cannot be remedied by the Board’s general conclusions about what is “basic knowledge” or “common sense.”” In re Lee, 61 USPQ2d 1430, 1432-1433 (Fed. Cir. 2002), quoting In re Zurko, 59 USPQ2d 1693, 1697 (Fed. Cir. 2001). Should the Examiner maintain the rejection after considering the arguments presented herein, Applicant submit that the Examiner must provide “the explicit basis on which the examiner regards the matter as subject to official notice and [allow Applicant] to challenge the assertion in the next reply after the Office action in which the common knowledge statement was made” (Id. at 3, emphasis in original), or else withdraw the rejection.

Further to demonstrating that combining the teachings of Sakui et al. with those of Komiyama would not have resulted in Applicant’s claimed invention, Applicant respectfully submits that Sakui et al., in fact, teaches away from such a combination. In particular, Sakui et al. discloses a plurality of semiconductor chips of the *same structure*

stacked one on another, and option circuits of each semiconductor chip are selected in accordance with the connecting pattern of the metal bumps provided between semiconductor chips. Id. at col. 5, lines 14-19 (emphasis added). Therefore, it would be inconsistent with the teachings of Sakui et al. to incorporate the teachings of Komiyama, which discloses an IC chip 2 mounted in flip-chip configuration and protruded electrodes 49 provided at specified portions of the conductive pattern 47, and are respectively connected to the protruded electrodes 24 formed on a main surface of the IC chip 2. Id. at col. 5, lines 1-11 and Fig. 4. In view of such teachings away, neither is there any motivation to combine the teachings of the references to result in the claimed invention, nor is there any reasonable expectation of success from doing so.

In summary, the Examiner has failed to establish a *prima facie* case of obviousness for claim 3. Accordingly, Applicant requests the Examiner to withdraw the rejection of claim 3 under 35 U.S.C. § 103(a) and the claim be allowed. Applicant submits that claims 12, 13, and 19 are also allowable at least in view of their dependency from allowable claim 3.

III. Claims 20 and 25 (Sakui et al., Iijima et al., and Hsuan et al.)

Claims 20 and 25 contain recitations similar to claims 3 and 21.

Specifically, claim 20 recites, *inter alia*, “one of the first connecting terminals and the second connecting terminals are arranged to be closer to [an] assembly board and the average density of arrangement of the one of the first connecting terminals and the second connecting terminals is lower than that of another of the first connecting terminals and the second connecting terminals.”

As discussed above regarding the rejection of claim 3, Sakui et al. and Iijima et al. either taken alone or in combination, do not teach or suggest at least the quoted element.

Hsuan et al., cited merely in an attempt to show chips of different sizes, does not cure these deficiencies of Sakui et al. and Iijima et al. Therefore, Sakui et al., Iijima et al., and Hsuan et al., either taken alone or in combination, do not teach or suggest each and every element of claim 20.

Claim 25 recites a semiconductor device comprising, among other things, “some of the first connecting terminals or the second connecting terminals is distributed and arranged substantially on an entire surface of the semiconductor chip, and power source supply potential or ground potential is to be applied to said some of the first or second connecting terminals.”

As discussed above regarding the rejection of claim 21, Sakui et al. does not teach or suggest at least “some of the first connecting terminals or the second connecting terminals is distributed and arranged substantially on an entire surface of the semiconductor chip, and power source supply potential or ground potential is to be applied to said some of the first or second connecting terminals,” as recited in claim 25.

Iijima et al., cited merely for a flip chip device, and Hsuan et al., cited merely for chips of different sizes, do not cure these deficiencies of Sakui et al. Therefore, Sakui et al., Iijima et al., and Hsuan et al., either taken alone or in combination, do not teach or suggest each and every element of claim 25.

Further, there is no motivation to combine the teachings of the cited references. As discussed above, there is no motivation to combine the teachings of Sakui et al. with

those of Iijima et al. In addition, contrary to the Examiner's allegations and conclusions, there is no motivation to combine the teachings of Hsuan et al. with those of Sakui et al. Further to demonstrating that combining the teachings of Sakui et al. with those of Iijima et al. and Hsuan et al. would not result in Applicant's claimed invention, Applicants respectfully submit that Sakui et al., in fact, teaches away from such a combination. In particular, Sakui et al. discloses a plurality of semiconductor chips of the *same structure* stacked one on another, and option circuits of each semiconductor chip are selected in accordance with the connecting pattern of the metal bumps provided between semiconductor chips. Id. at col. 5, lines 14-19 (emphasis added). Therefore, it would be inconsistent with the teachings of Sakui et al. to incorporate chips of different sizes, as taught by Hsuan et al. into the device of Sakui et al. At least absent such motivation, clearly there would be no reasonable expectation of success.

Therefore, the Examiner has failed to establish a *prima facie* case of obviousness for claims 20 and 25. Accordingly, Applicant requests the Examiner to withdraw the rejection of claims 20 and 25 under 35 U.S.C. § 103(a) and the claims allowed.

Conclusion

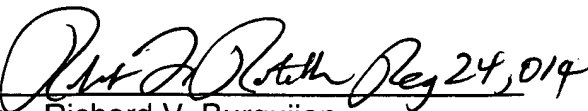
In view of the foregoing remarks, Applicant respectfully requests reconsideration and reexamination of this application and the timely allowance of the pending claims.

Please grant any extensions of time required to enter this response and charge any additional required fees to our deposit account 06-0916.

Respectfully submitted,

FINNEGAN, HENDERSON, FARABOW,
GARRETT & DUNNER, L.L.P.

Dated: March 2, 2004

By:  Reg 24,014
For Richard V. Burgujian
Reg. No. 31,744